| Discipline      | DIGITAL LOGIC                                                                                                  | code: 09 | summer semester |
|-----------------|----------------------------------------------------------------------------------------------------------------|----------|-----------------|
| Specialty       | Computer Systems and Technologies                                                                              |          |                 |
| ECTS credits: 7 | Form of assessment: exam                                                                                       |          |                 |
| Lecturer        | Assoc. Prof. Yulka Petkova, PhD<br>Room 207-3 E<br>Phone: +359 52 383 403<br>E-mail: yulka.petkova@tu-varna.bg |          |                 |
| Department      | Computer Science and Engineering                                                                               |          |                 |
| Faculty         | Faculty of Computing and Automation                                                                            | n        |                 |

Learning objectives:

The course is oriented towards the fundamental preparation of the students of the specialty "CST" at TU - Varna. The aim is to give the students knowledge and skills in the methods of analysis and synthesis of logic circuits and their use in computer systems and technologies. The main objectives of the discipline are related to the formation of knowledge and skills in the students: presentation and minimization of logical functions; methods for analysis and synthesis of combinational logic circuits; methods for analysis and synthesis of sequential logical circuits; microprogramming machines and their applications; programmable logic devices and their use in the synthesis of logic circuits.

| CONTENTS:                                                                                 |    |                               |
|-------------------------------------------------------------------------------------------|----|-------------------------------|
| Training Area                                                                             |    | Hours<br>seminar<br>exercises |
| Presentation and minimization of logic functions                                          |    | 5                             |
| Methods for analysis and synthesis of combinational logic circuits                        |    | 5                             |
| Methods for analysis and synthesis of sequentional logic circuits (Finite State Machines) |    | 5                             |
| Counters and Shift registers                                                              |    | 5                             |
| Microprogramming state machines and their applications                                    |    | 5                             |
| Programmable logic devices and their use in the synthesis of logic circuits               |    | 5                             |
| TOTAL: 60 h                                                                               | 30 | 30                            |